

REMARKS

Claims 52 through 54 are currently pending in the application.

Claims 52 through 54 were previously rejected. Applicants respectfully request reconsideration of the application.

**Abstract**

The Abstract was objected to by the Examiner for proper language and format. Applicants have amended the Abstract to clarify the embodiments of the presently claimed invention and to conform to the language requirements of M.P.E.P. § 608.01 (b). Applicants respectfully request withdrawal of the objection to the Abstract.

**Information Disclosure Statement**

Applicants have attached a copy of the Supplemental Information Disclosure Statement filed on January 24, 2002. Also attached is the date stamped return receipt postcard showing receipt of the IDS on February 7, 2002. Applicants respectfully request that the documents cited on the PTO-1449 be made of record herein.

**35 U.S.C. § 102(b) Anticipation Rejections**

Anticipation Rejection Based on U.S. Patent 5,067,233 to Solomon

Claims 52 and 54 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Solomon, (U.S. Patent 5,067,233). Applicants respectfully traverse this rejection as hereinafter set forth.

Applicants submit that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 UWPQ2d 1051, 1053 (Fed Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Solomon describes a method of forming integrated circuit modules suitable for supporting arrays of infrared detector elements in a space environment. (Col. 1, lines 10-13). The

edges of the preferred embodiment are beveled, using anisotropic etching of the surfaces of single crystalline silicon integrated circuit layers. Both the layer and the contact board are formed to have crystalline lattice structures oriented to complement one another. (Col. 2, lines 38-46).

FIG. 1 shows that the layer 11 is formed to have a beveled edge 15, while contact board 13 is formed to have a beveled edge 17 shaped to mate with beveled edge 15 on layer 11. (FIG. 1). The shape of the beveled edge is created by anisotropic etching which etches in a predictable direction, with the angle being determined by the silicon crystal lattice. (Col. 4, lines 1-11).

FIG. 2A illustrates and the specification associated therewith describes a contact board 13 formed to include conductive pads 21 formed on the beveled surface 17. The layers 11 are formed to include conductive pads 23 which abut contact board pads 21. The layer conductive pads are in electrical contact with conductive pattern 25, formed on layer 11. Conductive pattern 25 relays signals from conductive pad 23 to integrated circuit structure formed in the surface of layer 11. (Col. 4, lines 34-44).

By way of contrast with the cited prior art Solomon reference, claim 52 as presently claimed recites "a socket contact formation process, comprising: forming a contact head from a conductive material; forming a contact body from a semiconductive material configured to be electrically conductive; and joining said contact head and said contact body." A socket contact is materially different from an integrated circuit module layer. A socket contact is designed to form a single electrical connection as part of a larger integrated circuit device. Solomon is specifically directed toward forming multiple electrical contact layers as part of a larger integrated circuit module and is more specifically directed toward infrared detector arrays. One electric contact is created by abutting board 11 against contact board 13. Depending on the design, multiple contacts may be made through contact pads on boards 11 and 13. Another electrical communication in Solomon is created by metal-filled conductive vias that connect the beveled and straight edges of contact board 13. These vias are electrically connected through integrated circuit structure 27, which electrically connects the multiple layers forming the integrated circuit module. Furthermore, the vias of the presently claimed invention are formed by a semiconductor material configured to be electrically conductive and not by vapor deposition as in Solomon. Each and every element of claim 52 is not found either expressly or inherently in the disclosure

of Solomon. In particular, Solomon does not disclose “forming a contact body from a semiconductive material configured to be electrically conductive”.

As Solomon fails to expressly or inherently teach every element of claim 52, Applicants submit that claim 52 is not anticipated by Solomon under 35 U.S.C. § 102. Therefore, claim 52 is allowable.

Claim 54 is allowable as depending, either directly or indirectly from allowable claim 52.

### 35 U.S.C. § 103(a) Obviousness Rejections

#### Obviousness Rejection Based on U.S. Patent 5,067,233 to Solomon

Claim 53 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Solomon (U.S. Patent 5,067,233).

Applicants submit that:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference of combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference) or references when combined must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant’s disclosure.

The discussion of Solomon above is incorporated by reference. By way of contrast with the cited prior art Solomon reference, claim 53 recites a process wherein “said step of forming a contact head comprises stamping a metal element; said step of forming a contact body comprises etching silicon; and said step of joining said contact head and said contact body further comprise adhering said contact head onto said contact body.” Solomon does not teach or suggest all the claim limitations of claim 53 to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. More specifically, at the least, Solomon fails to teach or suggest forming a socket contact by joining a contact head made of a conductive material with a contact body made of a semiconductive material configured to be electrically conductive. Solomon discloses electrical communication between metal surfaces using metal filled

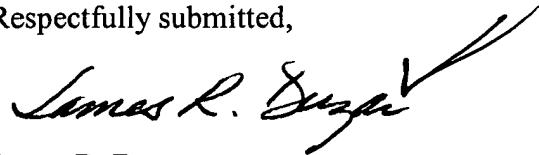
conductive vias. Solomon teaches away from stamping a metal element since metal layer 27 is an integrated circuit layer, which is formed on the upper surface of wafer 52. (Col. 6, lines 9-12). Solomon discloses that layer 27 is formed, not stamped and also that the vias 31 are filled by metal film deposition. (Col. 5, lines 52-54). Additionally, given the small size of the structures taught by Solomon stamping would not be obvious to try, since controlling tolerances would be more difficult. Therefore, Solomon teaches away from using stamping.

As Solomon fails to teach or suggest every element of claim 53 and it would not be obvious to combine the teachings of Solomon with metal stamping to establish a *prima facie* case of obviousness regarding the claimed invention under 35 U.S.C. § 103.

Claim 53 is also allowable as depending from allowable claim 52.

Claims 52 through 54 are allowable over the cited prior art. The Abstract has been amended as requested to only cite the embodiment of the invention set forth in claims 52 through 54 of the application

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Date: January 15, 2003

JRD/sls:djp

Enclosure: Version with Markings to Show Changes Made

Document in ProLaw

**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**IN THE SPECIFICATION:**

A marked-up version of the Abstract, highlighting the changes thereto, follows to clearly identify the amendments:

In a socket [used] to [house] test semiconductor die [during testing], a recessed socket contact and methods of making [the same are provided] contacts that avoid pinching the die [die's] contacts are disclosed. [Also provided are socket contacts and methods of making the same that allow for smaller socket holes and, therefore, denser arrays of socket contacts.] The socket contacts allow for smaller socket holes and allow denser contact spacing. [In one embodiment, the body of the socket contact comprises a head, a spring coupled to the head, and a shaft coupled to the spring; no outer shell is needed for the spring, as the non-conductive sides of the socket hole serve that function. In another embodiment, the body of the socket contact comprises a metal shaft having an aperture. Compression causes the shaft to buckle at the slit, thereby decreasing the amount of lateral buckling.] In an [yet another] embodiment, semiconductor fabrication techniques are used to construct a dense array of contacts. A socket contact formation process comprises forming a contact head from a conductive material, forming a contact body from a semiconductive material configured to be electrically conductive; and joining said contact head and said contact body.